UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,966	03/31/2000	Stephen D. Macarthur	07072-101001	2142

45456 7590 08/24/2004	EXAMINER
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ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/539,966	MACARTHUR, STEPHEN D.
	Examiner	Art Unit
	Mike Nguyen	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _05/10/2004_.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-31_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-31_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _5/10/04 & 06/18/04_. ●

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.   Applicant's amendment file on 05/10/2004 in response to Examiner's Office Action has

been reviewed but they are not deemed to be persuasive. The following rejections now apply.

2.   Claims 1-31 are pending for the examination.

Drawings

3.   This application has been filed with informal drawings which are acceptable for

examination purposes only. Formal drawings will be required when the application is allowed.

Double Patenting

4.   The nonstatutory double patenting rejection is based on a judicially created doctrine
grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or
improper timewise extension of the "right to exclude" granted by a patent and to prevent possible
harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.
Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686
F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA
1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).
        A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to
overcome an actual or provisional rejection based on a nonstatutory double patenting ground
provided the conflicting application or patent is shown to be commonly owned with this
application. See 37 CFR 1.130(b).
        Effective January 1, 1994, a registered attorney or agent of record may sign a terminal
disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37
CFR 3.73(b).

5.   Claims 1-31 are provisionally rejected under the judicially created doctrine of

obviousness-type double patenting as being unpatentable over claims 1-75 of copending

Application No. 09/540,828. Although the conflicting claims are not identical, they are not

patentably distinct from each other because it would have been obvious to be not grouped "a

plurality of first directors" and "a plurality of second directors" into "a plurality of first director

boards" and "a plurality of second director boards" in the system interface, or the data storage

system in order to provide more reliable in transferring data of system interface and to protest

against total system failure in the event of a failure in a component or subassembly of the storage

system. In addition, it would have been obvious to put "a switch" in either the boards or the

message network or both in order to provide same motivation as above.

6.   Claims 1-31 are rejected under the judicially created doctrine of obviousness-type double

patenting as being unpatentable over claims 1-2, 5-6 and 9-10 of U.S. Patent No. 6,651,130 B1.

Although the conflicting claims are not identical, they are not patentably distinct from each other

because it would have been obvious to be not grouped "a plurality of first directors" and "a

plurality of second directors" into "a plurality of first director boards" and "a plurality of second

director boards" in the system interface or the data storage system in order to provide more

reliable in transferring data of system interface and to protest against total system failure in the

event of a failure in a component or subassembly of the storage system. In addition, it would

have been obvious to include "a common bus, such as interconnecting the data pipe, the

microprocessor, and the controller" in order to provide same motivation as above.

7.   This is a provisional obviousness-type double patenting rejection because the conflicting

claims have not in fact been patented.

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

9.   Claims 1-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin et al.

(U.S. Pat. No. 5,214,768) in view of Gaskins (U.S. Pat. No. 5,903,911).

As to claim 1, Martin teaches a system interface comprising:

(a)   a plurality of first director boards (it is inherently to combine a plurality of first directors

(figure 1 elements 14, 16, 18, 19) into a plurality of director boards), each one of the first director

boards having:

(i) a plurality of first directors (see figure 1 elements 14, 16, 18, 19 and column 5 lines

20-30); and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one

of the first director boards and a pair of output/input ports (see figures 2A, 3 element 122 and

column 10 line 46 to column 11 line 25);

(b)   a plurality of second director boards (see figure 1 element 56 and column 5 lines 53-58),

each one of the second directors boards having:

(i) a plurality of second directors (see figure 1 element 48 and column 5 lines 49-58); and

(ii) a crossbar switch having input/output ports coupled to the second directors on such

one of the second director boards and a pair of output/input ports (see figure 2B element 48 and

figure 8);

(c)   a data transfer section coupled to the plurality of first and second directors (see figure 2

element 42 and column 7 lines 25-34 and column 14 lines 4-18);

(d)   a message network coupled to the pair of output/input ports of each one of the directors

boards of the plurality of the first director boards and to the pair of output/input ports of each one

of the directors boards of the plurality of second director boards (see figures 5, 6 and column 14

lines 37-45 figure 2 element 42 and column 7 lines 25-34 and column 14 lines 4-18); and

Although the system interface taught by Martin shows substantial features of the claimed

invention (discussed above), it fails to explicitly teach: a cache memory, the message network

operative independently of the data transfer section, and wherein the first and second directors

control data transfer between the first directors and the second directors in response to messages

passing between the first directors and the second directors through the message network to

facilitate data transfer between first directors and the second directors with such data passing

through the cache memory in the data transfer section. Gaskins; however, teaches a cache

memory (see figure 2 element 206), the message network operative independently of the data

transfer section (see figure 2 element 208), and wherein the first and second directors control

data transfer between the first directors and the second directors in response to messages passing

between the first directors and the second directors through the message network to facilitate

data transfer between first directors and the second directors with such data passing through the

cache memory in the data transfer section (see figures 3, 4 and column 9 lines 10-65). Given the

teaching of Gaskins, a person having ordinary skill in the art would have readily recognized the

desirability and advantages of modifying Martin by employing the well known or conventional

feature of the system interface, such as taught by Gaskins, in order to provide increasing the

bandwidth of the data transfer section (see column 4 lines 39-52).

As to claim 2, Martin teaches the system interface recited in claim 1 wherein each one of

the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache

memory (see figure 3 and column 10 lines 56-62);

Although the system interface taught by Martin shows substantial features of the claimed invention (discussed above), it fails to explicitly teach: a controller. Gaskins; however, teaches a controller for transferring the messages between the message network and such one of the first directors (see column 9 lines 12-14, 41-43). Given the teaching of Gaskins, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Martin by employing the well known or conventional feature of the system interface, such as taught by Gaskins, in order to provide increasing the bandwidth of the data transfer section (see column 4 lines 39-52).

As to claims 3 and 4, Martin teaches the system interface wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory (see figure 8 element 316 and column 15 lines 62-66);

Although the system interface taught by Martin shows substantial features of the claimed invention (discussed above), it fails to explicitly teach: a controller. Gaskins; however, teaches a controller for transferring the messages between the message network and such one of the second directors (see column 9 lines 21-30, 45-65). Given the teaching of Gaskins, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Martin by employing the well known or conventional feature of the system interface, such as taught by Gaskins, in order to provide increasing the bandwidth of the data transfer section (see column 4 lines 39-52).

As to claim 5, Martin teaches the system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache a memory (see figure 3 and column 10 lines 56-62);

a microprocessor (see figure 3 elements 124, 126, 128); and

Although the system interface taught by Martin shows substantial features of the claimed invention (discussed above), it fails to explicitly teach: a controller. Gaskins; however, teaches a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory (see column 9 lines 12-30, 41-65). Given the teaching of Gaskins, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Martin by employing the well known or conventional feature of the system interface, such as taught by Gaskins, in order to provide increasing the bandwidth of the data transfer section (see column 4 lines 39-52).

As to claims 6 and 7, Martin teaches the system interface wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory (see figure 8 element 316 and column 15 lines 62-66);

a microprocessor (see figure 8 element 318); and

Although the system interface taught by Martin shows substantial features of the claimed

invention (discussed above), it fails to explicitly teach: a controller. Gaskins; however, teaches a

controller coupled to the microprocessor and the data pipe for controlling the transfer of the

messages between the message network and such one of the second directors and for controlling

the data between the input of such one of the second directors and the cache memory (see

column 9 lines 12-30, 41-65). Given the teaching of Gaskins, a person having ordinary skill in

the art would have readily recognized the desirability and advantages of modifying Martin by

employing the well known or conventional feature of the system interface, such as taught by

Gaskins, in order to provide increasing the bandwidth of the data transfer section (see column 4

lines 39-52).

Claim 8 is of similar scope as claim 1 and is therefore rejected under same rationale.

Martin also teaches a data storage system for transferring data between a host computer/server

and a bank of disk drives through a system interface (see figure 1 elements 12, 44).

Claims 9-14 are of similar scope as claims 2-7 and are therefore rejected under same

rationale.

Claim 15 is of similar scope as claim 1 and is therefore rejected under same rationale.

Martin also teaches the data transfer section is also coupled to output/input port of the crossbar

switch of each one of the plurality of first director boards and to the output/input port of the

crossbar switch of each one of the plurality of second director boards (see figure 7 and column 14 lines 4-26).

Claims 16-21 are of similar scope as claim 2-7 and are therefore rejected under same rationale.

Claim 22 is of similar scope as claim 8 and is therefore rejected under same rationale. Martin also teaches the data transfer section is also coupled to output/input port of the crossbar switch of each one of the plurality of first director boards and to the output/input port of the crossbar switch of each one of the plurality of second director boards (see figure 7 and column 14 lines 4-26).

Claims 23-28 are of similar scope as claims 2-7 and are therefore rejected under same rationale.

Claim 29 is of similar scope as claim 22 and is therefore rejected under same rationale. Martin also teaches a data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface (see figure 1 elements 12, 44).

As to claim 30, Martin teaches a system interface comprising:

(a)   a plurality of first director boards (it is inherently to combine a plurality of first directors

(figure 1 elements 14, 16, 18, 19) into a plurality of director boards), each one of the first director

boards having:

(i) a plurality of first directors (see figure 1 elements 14, 16, 18, 19 and column 5 lines

20-30); and

(ii) a crossbar switch having input/output ports coupled to the first directors on such one

of the first director boards and a pair of output/input ports (see figures 2A, 3 element 122 and

column 10 line 46 to column 11 line 25);

(b)   a plurality of second director boards (see figure 1 element 56 and column 5 lines 53-58),

each one of the second directors boards having:

(i) a plurality of second directors (see figure 1 element 48 and column 5 lines 49-58); and

(ii) a crossbar switch having input/output ports coupled to the second directors on such

one of the second director boards and a pair of output/input ports (see figure 2B element 48 and

figure 8);

(c)   a data transfer section coupled to the data ports of the plurality of first and second

directors (see figure 2 element 42 and column 7 lines 25-34 and column 14 lines 4-18);

(d)   a message network coupled to the pair of output/input ports of each one of the directors

boards of the plurality of the first director boards and to the pair of output/input ports of each one

of the directors boards of the plurality of second director boards (see figures 5, 6 and column 14

lines 37-45 figure 2 element 42 and column 7 lines 25-34 and column 14 lines 4-18); and

Although the system interface taught by Martin shows substantial features of the claimed

invention (discussed above), it fails to explicitly teach: each one of the directors having a data

port and a message port, a cache memory, and wherein the first and second directors control data

transfer between the first director and the second director with data in such data transfer passing

through the cache memory in response to messages passing between the first director and the

second director through the message network. Gaskins; however, teaches each one of the

directors having a data port and a message port (see figure 2 and column 7 lines 5-14), a cache

memory (see figure 2 element 206), and wherein the first and second directors control data

transfer between the first director and the second director with data in such data transfer passing

through the cache memory in response to messages passing between the first director and the

second director through the message network (see figures 3, 4 and column 9 lines 10-65). Given

the teaching of Gaskins, a person having ordinary skill in the art would have readily recognized

the desirability and advantages of modifying Martin by employing the well known or

conventional feature of the system interface, such as taught by Gaskins, in order to provide

increasing the bandwidth of the data transfer section (see column 4 lines 39-52)

Claim 31 is of similar scope as claim 1 and is therefore rejected under same rationale.

Gaskin also teaches each one of the messages includes a destination field (see column 7 lines 66-

67).

Response to Amendment

10.   In response to the applicant's arguments that "However, element 208 is a CACHE

MEMORY CONTROLLER not a message network operative independently of the data transfer

section and wherein the first and second directors control data transfer between the first and

second directors in response to messages passing between the first and second directors through

the message network". Examiner disagrees, in figs 3, 34 and column 9 lines 10-65 (as indicated

in the Office Action mailed 01/09/2004), clearly indicates that the cache memory controller

handles a read/write request and it operates independently of the cache memory which handles

data transfer.

In response to the applicant's arguments that "Applicants fails to see ... where messages

by-passing the data transfer section or is operative independently of the memory increases the

bandwidth of the system". Examiner disagrees, in column 4 lines 39-52, clearly indicates that to

increase the bandwidth of the system a prefetch technique may be employed. In this prefetch

technique, the cache controller is used to handle the read/write request and the cache memory is

used to handle data.

In response to the applicant's arguments that "... Gaskins does not describe that

messages passing through the message network have a destination field". Examiner disagrees, in

column 7 line 65 to column 8 line 6, clearly indicates that a physical address signal (destination

field) is provided to comparator 302 of the cache memory controller.

Conclusion

11.   Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this
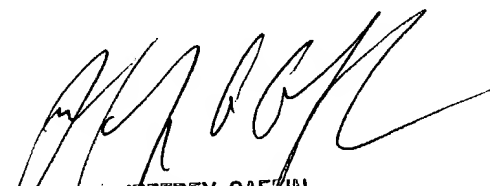
final action.

12.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Mike Nguyen whose telephone number is 703 305-5040. The

examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Jeffrey Gaffin can be reached on 703 308-3301. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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TECHNOLOGY C--- --100

08/19/2004